of said sealed cavity not directly above said microstructure;

introducing a non-liquid etchant into said sealed cavity through said one or more holes using a barrel etcher, said structural material and said sacrificial material having a high etch rate differential with respect to said etchant, such that said sacrificial material is removed; and

sealing said one or more holes in said sealed cavity.

- Please delete claim 23.

REMARKS

The Examiner has rejected claim 23 under 35 U.S.C. § 112 first paragraph. stating that claim 23 contains subject matter not supported by the specification. In response, the Applicant has deleted claim 23.

The Examiner has rejected Claims 1-2, 4 and 21-23 under 35 U.S.C. §103(a) as being unpatentable over the Applicant's admitted prior art (APA), in view of U.S. Patent 5,578,976 (Yao). The Applicant's APA, as well as the previously cited Muller, et al. reference, both disclose the fabrication of a micro-structure in a sealed cavity using a wet etch process. The Yao reference discloses a method of forming a mems structure, wherein a barrel etcher is used to deliver dry oxygen plasma etchant to remove sacrificial layers to circumvent problems associated with striction. In addition, U.S. Patent 5,083,857 (Hornbeck) discloses the removal of sacrificial layers using a dry oxygen plasma etch.

The Examiner states that it would have been obvious to one of ordinary skill in the art at the time invention was made to use the barrel etcher and the oxygen plasma etchant to remove the sacrificial layers from the aluminum structural material. The Applicant respectfully disagrees with this conclusion.

First, it is noted that the Applicant is using a dry oxygen plasma etch to release a microstructure within a sealed cavity. No combination of the prior art cited by the Examiner shows the removal of sacrificial layers within a sealed cavity by use of an oxygen plasma etch. Conventional wisdom in the art at the time of the application provided for the removal of the sacrificial layer within a sealed cavity by means of a wet etch. There are several reasons why it was not thought possible to use a dry etch within a sealed cavity to remove the layers of sacrificial material.

First, the behavioral characteristics of the dry etchant, while well understood when used in unconfined areas, are not well known or understood when used in a sealed cavity environment, wherein access is restricted and etch distances are relatively large.

When etching the sacrificial layers within a sealed cavity, it is necessary to place the access holes for introduction of the etchant into the sealed cavity in areas that are not directly above the microstructure itself. This is because when the holes in the cap forming the sealed cavity are filled after the removal of the sacrificial layers, it is undesirable to have the material used to fill the holes also being deposited on areas of the microstructure itself, because this would change the characteristics of the microstructure and may even prevent the microstructure from being able to move. This restricts the area for possible placement of access holes to the outermost edges of the cap and the sides of the cap. For this reason, it is thought that a dry etch could not be used within the sealed cavity because of the extremely long distances which need to be etched to remove the sacrificial layer from the entire area underneath and on top of the microstructure.

In support of this, the Applicant brings the Examiner's attention to Exhibit A, attached hereto, which is an excerpt from a book entitled, *Fundamentals of Microfabrication*, Madou, CRC Press (1997) On page 234, the Applicant has underlined a section of text which talks about selective removal of the spacer layer from the underside of a microstructure. The text states:

> Commonly, a layer of sacrificial phosphosilicate glass, between 1000 and 2000 μm long and 0.1 to 5 μm thick is etched in concentrated, dilute or buffered HF. The spacer etch rate R_s should be faster than the attack on the microstructural element R_m and that of the insulator layer R_i. *For this type of complete undercutting, only wet etchings can be used. Etching narrow gaps and undercutting wide areas with BHF can take hours. To shorten the etch time, extra apertures in the microstructures sometimes are provided for additional access to the spacer layer.*

(emphasis added).

This article shows that the low etch rate and therefore, the long etch time required to remove the spacer layer underneath the microstructure was believed to make it uneconomical to remove the spacer layer in this manner.

The fact that the access holes in the cap forming the sealed cavity must be placed near the edges thereof result in the oxygen plasma dry etchant forming tunnels into the sacrificial layers which are separating the microstucture from the cap and substrate.

These long tunnels have very high aspect ratios (defined as the depth of the etching divided by the size of the opening) which results in extremely low etch rates. Extremely low etch rates can be attributed in these instances to the difficulty in removing the by-products of the etch process to allow fresh etchant to enter the area. The Applicant brings the Examiner's attention to Exhibit B, attached hereto, which is an excerpt from the *Handbook of Microlithography, Micromachining, and Microfabrication,* Rai-Choudhury, Ed., SPIE Optical Engineering Press (1997). On page 115, a graph is presented showing the aspect ratio versus the average etch rate in nm/min. The graph clearly shows that the etch rate falls as the trench aspect ratio grows and in fact, the graph shows the trench aspect ratio up to 35. The Applicant notes that it is possible using the Applicant's process to etch tunnels into the sacrificial layers having aspect ratios of 100 to 150, which would provide an extremely low average etch rate. The fact that the graph only show etch rates up to 35 indicated that etch rates in the Applicant's range were out of the scope of what was known in the prior art.

The Applicants further direct the Examiner's attention to Exhibit C attached hereto, which is an excerpt from a book entitled, *Electronic Materials Chemistry*, H. B. Pogge, Ed., Marcel Decker, Inc. (1996). On page 292 a similar graph is shown giving aspect ratio versus normalized etch rate, again showing the etch rate as a function of the aspect ratio wherein the etch rate falls and the aspect ratio increases. Once again, this graph only shows an aspect ratio of up to 25, whereas the Applicant is using the process to etch tunnels with aspect ratios of between 100 and 150.

The extremely low etch rate is also made worse by the use of the barrel etcher. The Applicant directs the Examiner's attention to Exhibit D, attached hereto, which is an excerpt from a book entitled, *Dry Etching for Microelectronics*, R. A. Powell, Ed., North-Holland Physics Publishing (1984). On page 121, there is table comparing operating characteristics of various dry etch techniques. You will see that the barrel etch is performed at a pressure of between 100 and 1,000 mTorr. If you will refer back to Exhibit B, on page 114, there is graph of etch rate versus spacing between elements as a function of pressure. You will see that at 3 mTorr the line is relatively flat while at 50 mTorr the line drops off precipitously. The barrel etcher etches at pressures between 100 and 1,000 mTorr, which would imply a worsening effect on the etch rate through the substance.

The Applicant has shown conventional wisdom at the time of the invention taught away from the use of the dry etchant in a sealed cavity to remove large areas of sacrificial material underneath and on top of a microstructure within the sealed cavity because of the

extremely low etch rate. The extremely low etch rate is a by-product of the required placement of the holes to avoid depositing material on the microstructure when the holes in the cap are sealed. It was therefore thought the wet etch was the only means economically feasible to remove the sacrificial layer underneath the microstructure, especially with larger sized microstuctures.

The Applicant is not concerned about the long time required to remove the sacrificial layers because multiple units can be etched at one time when the barrel etcher is used. For a single unit in a parallel plate type etcher, the long time required to remove the sacrificial layers using dry etch would make the process uneconomical. However, when dozens of units can be etched at the same time in the barrel etcher, the etching time per unit drops and the practice becomes economical. Additionally, the choice of materials is important. It is necessary to select materials which tend to not absorb the reactants of the etching process to make it easier to move etchant into the areas deep into the tunnels.

The Applicants have modified claim 1 of the Application to make it clear that the entire sacrificial layer which underlies the microstucture and the entire sacrificial layer upon which the cap is formed are removed in one step using the dry etch process. The fact that these layers can be removed in a one-step dry etch process is an improvement over the prior art. In the prior art, it would have been required to form stand-offs of sacrificial material on the top and bottom of the microstructure and to remove the remaining sacrificial material using a wet etchant, followed by a dry etch step to remove the stand-offs to prevent problems associated with striction. Therefore, it can be seen that the current process saves three steps in the manufacturing cycle, namely that of creating holes in the original sacrificial layers, depositing stand-offs in the above mentioned holes out of a material that would not be attacked readily by the wet etchant used to remove the rest of the sacrificial layers, and then another step to remove the standoffs.

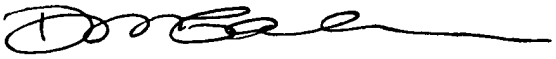
The Applicant has further modified claim 1 to make it clear that the access holes in the cap of the sealed cavity should not be above the microstructure, itself, thereby implying that the etching tunnels will have large aspect ratios, resulting in extremely low etch rates.

CONCLUSION

The Applicant has modified claim 1 and has provided evidence that it would not have been obvious to combine the references cited by the Examiner according to the conventional wisdom in the art at the time of the filing of the Application. Therefore, the Applicant

respectfully submits that the Examiner's combination of the references and the rejection under § 103(a) based thereon has been traversed and that the Application as amended is in condition for immediate allowance. The Applicant therefor requests that the Examiner allow the Application at the earliest possible time, based on the amendments and remarks herein.

Respectfully submitted,



Dennis M. Carleton
Reg. No. 40,938
Buchanan Ingersoll, P.C.
One Oxford Centre, 20th Floor
Pittsburgh, PA 15219
(412) 562-1895
e-mail: carletondm@bipc.com

Dated: April 30, 2002

Attorney for Applicant

ADDENDUM
(Marked Up Claims)

1. (Amended) A method of fabricating a microstructure in a sealed cavity comprising the steps of :

providing a substrate;

forming a microstructure composed of a structural material on said substrate [in a sealed cavity,] said microstructure being secured to said substrate [at one or more points by a sacrificial material] by a first layer of sacrificial material;

forming a second layer of sacrificial material on said microstructure;

forming a cap on said second layer of sacrificial material, said cap forming a sealed cavity containing said microstructure and said first and said second sacrificial layers.

forming one or more holes in said sealed cavity, said holes being restricted to an area of said sealed cavity not directly above said microstructure ;

introducing a non-liquid etchant into said sealed cavity through said one or more holes using a barrel etcher, said structural material and said sacrificial material having a high etch rate differential with respect to said etchant, such that said sacrificial material is removed; and

sealing said one or more holes in said sealed cavity.

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Fundamentals of MICROFABRICATION

Marc Madou

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and sheet resistance uniformity less than 2%. Alternatively, poly-Si may be doped from PSG films sandwiching the undoped poly-Si film. By annealing such a sandwich at 1050°C in N_2 for one hour, the polysilicon is symmetrically doped by diffusion of dopant from the top and the bottom layers of PSG. Symmetric doping results in a polysilicon film with a moderate compressive stress. The resulting uniform grain texture avoids gradients in the residual stress which would cause bending moments warping microstructures upon release. Finally, ion implantation of undoped polysilicon, followed by high temperature dopant drive-in, also leads to conductive polysilicon. This polysilicon has a moderate tensile stress, with a strain gradient that causes cantilevers to deflect toward the substrate.[53] The poly-Si is now ready for patterning by RIE in, say, a CF_4-O_2 plasma.

Although the mechanical properties still are not well understood, microstructures based on poly-Si as a mechanical member have been commercialized.[19,55] Other structural materials used in surface micromachining include single crystal Si (epi-Si or etched back, fusion bonded Si), SiO_2, silicon nitride, silicon oxynitride, polyimide, diamond, SiC, GaAs, tungsten, α-Si:H, Ni, W, Al, etc. A few words about the merit of some of these materials as structural components follow.

Silicon nitride and silicon oxide also can be deposited by CVD methods but usually exhibit too much residual stress which hampers their use as mechanical components. However, CVD of mixed silicon oxynitride can produce substantially stress-free components.

Amorphous Si (α-Si) can be stress annealed at temperatures as low as 400°C.[75] This low-temperature anneal makes the material compatible with almost any active electronic component. Unfortunately, very little is known about the mechanical properties of amorphous Si.

Hydrogenated amorphous Si (α-Si:H), with its interesting electronic properties, is even less understood in terms of its mechanical properties. If the mechanical properties of hydrogenated amorphous Si were found as good as those of poly-Si, the material might make a better choice than poly-Si as a MEMS material given its better electronic characteristics.

Tungsten CVD deposition is IC compatible. The material has some unique mechanical properties (see Table 8.4). Moreover, the material can be applied selectively. Selective CVD tungsten has the unique property that tungsten will only nucleate on silicon or metal surfaces but does not deposit on dielectrics such as oxides and nitrides.[76]

Metals and polyimides, because they are easily deformed, usually do not qualify as mechanical members but have been used, for example, in plastically deformable hinges.[77,78] Aluminum constitutes the mirror material in Texas Instruments' flexure-beam micromirror devices (FBMDs). The metal is used both for the L-shaped flexure hinges and the mirror itself.[79] Polycrystalline diamond films, deposited by CVD, are potential high-temperature, harsh environment MEMS candidates.[80] Problems include oxidation above 500°C for nonpassivated films, difficulty of making reliable ohmic contact to the material, and the reproducibility and surface roughness of the films.[81] Poly-SiC films have been deposited by an APCVD process on four-inch, polysilicon-coated, silicon wafers. A surface micromachining process using the underlying polysilic n film as the sacrificial layer was developed. Poly-SiC is projected for use as structural material for high temperatures and harsh environments, and to reduce friction and wear between moving components.[82] Surface micromachining of thin single crystalline Si layers in SOI and with polyimides is discussed separately below.

Selective Etching of Spacer Layer

Selective Etching

To create movable micromachines the microstructures must be freed from the spacer layers. The challenge in freeing microstructures by undercutting is evident from Figure 5.16. After patterning the poly-Si by RIE in, say, a SF_6 plasma, it is immersed in an HF solution to remove the underlying sacrificial layer, releasing the structure from the substrate. Commonly, a layer of sacrificial phosphosilicate glass, between 1 and 2000 μm long and 0.1 to 5 μm thick, is etched in concentrated, dilute or buffered HF. The spacer etch rate, R_s, should be faster than the attack on the microstructural element, R_m, and that of the insulator layer, R_i. For this type of complete undercutting, only wet etchants can be used. Etching narrow gaps and undercutting wide areas with BHF can take hours. To shorten the etch time, extra apertures in the microstructures sometimes are provided for additional access to the spacer layer. The etch rate of PSG, the most common spacer material, increases monotonically with dopant concentration, and thicker sacrificial layers etch faster than thinner layers.[83]

The selectivity ratios for spacer layer, microstructure, and buffer layer are not infinite,[84] and in some instances even silicon substrate attack by BHF was observed under polysilicon/spacer regions.[85,86] Heavily phosphorous-doped polysilicon is especially prone to attack by BHF. Silicon nitride deposited by LPCVD etches much more slowly in HF than oxide films, making it a more desirable isolation film. When depositing this film with a silicon-rich composition, the etch rate is even slower (15 nm/min).[65] Eaton et al.[87] compared oxide and nitride etching in a 1:1 HF:H_2O and in a 1:1 HF:HCl solution and concluded that the HCl-based etch yielded both faster oxide etch rates (617 nm/min vs. 330 nm/min) and slower nitride etch rates (2 nm/min vs. 3.6 nm/min), providing a much greater selectivity of the oxide to silicon nitride (310 vs. 91!). The same authors also studied the optimum composition of a sacrificial oxide for the fastest possible etching in their most selective 1:1 HF:HCl etch. The faster sacrificial layer etch limited the damage to nitride structural elements. Their results are summarized in Table 5.3. A densified CVD SiO_2 was used as a control, and a 5%/5% borophosphosilicate glass (BPSG) was found to etch the fastest.

Watanabe et al.[88] using low pressure vapor HF, found high etch ratios of PSG and BPSG to thermal oxides of over 2000, with the BPSG etching slightly faster than the PSG. We will see further that low pressure vapor HF also leads to less stiction of structural elements to the substrate. In Table 5.4 we present etch rate and etch ratios for R_i and R_s in BHF (7:1) for a few selected materials.

Detailed studies on the etching mechanism of oxide spacer layers were undertaken by Monk et al.[83,89] They found that the

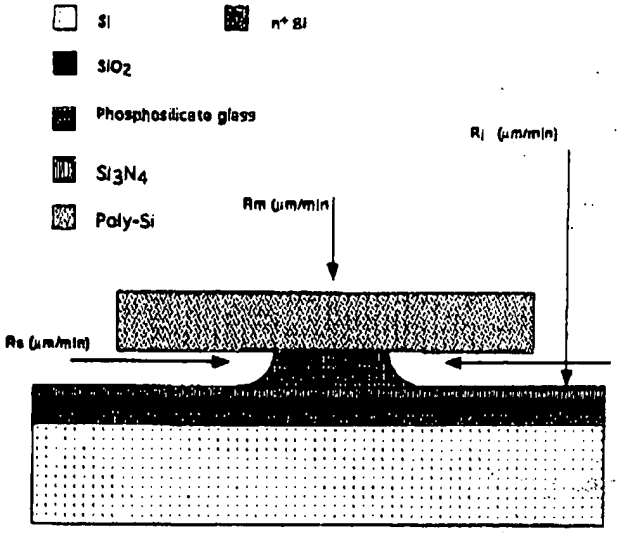

FIGURE 5.16 Selective etching of spacer layer.

TABLE 5.3 Etch Rate in 1:1 HF:HCl of a Variety of Sacrificial Oxides

Thin Oxide	Lateral Etch Rate (Å/min)
CVD SiO_2 (densified at 1050°C for 30 min)	6170
Ion-implanted and densified CVD SiO_2 (P, 8×10^{15}/cm², 50 keV)	8330
Phosphosilicate (PSG)	11,330
5%/5% borophosphosilicate (BPSG)	41,670

Source: Adapted from Eaton, W.P. and Smith, J.H., A CMOS-compatible, Surface Micromachined Pressure Sensor for Aqueous Ultrasonic Application, presented at SPIE Smart Structure and Materials, 1995.

TABLE 5.4 Etching of Spacer Layer and Buffer Layer in BHF (7:1)

	Material		
Property	LPCVD Si_3N_4	LPCVD SiO_2	LPCVD 7% PSG
Etch rate	7–12 Å/min (R_l)	700 Å/min (R_s)	~10,000 Å/min (R_s)
Selectivity ratio	1	60–100	~800–1200

etching reaction shifts from kinetic controlled to diffusion controlled as the etch channel becomes longer. This affects mainly large-area structures, as diffusion limitations were observed only after approximately 200 μm of channel etching or 15 min in concentrated HF. Eaton and Smith[90] developed a release etch model which is an extension of the work done by Monk et al.[83,89] and Liu et al.[91]

Etching is followed by rinsing and drying. Extended rinsing causes a native oxide to form on the surface of the polysilicon structure. Such a passivation layer often is desirable and can be formed more easily by a short dip in 30% H_2O_2.

Etchant-Spacer-Microstructure Combinations

A wide variety of etchant, spacer, and structural material combinations have been used; a limited listing is presented in Table 5.5. One interesting case concerns poly-Si as the sacrificial layer. This was used, for example, in the fabrication of a vibration sensor at Nissan Motor Co.[92] In this case poly-Si is etched in KOH from underneath a nitride/polysilicon/nitride sandwich cantilever. Also, a solution of HNO_3 and BHF can be used to etch poly-Si, but it proves difficult to control. Using aqueous solutions of NR_4OH, where R is an alkyl group, provides a better etching solution for poly-Si, with greater selectivity with respect to silicon dioxide and phosphosilicate glass. The relatively slow etch rate enables better process control[93] and the etchant does not contain alkali ions, making it more CMOS compatible. With tetramethylammonium hydroxide (TMAH) the etch rate of CVD poly-Si, deposited at 600°C from SiH_4, follows the rates of the (100) face of single crystal Si and is dopant dependent. The selectivity of Si/SiO_2 and Si/PSG, at temperatures below 45°C are measured to be about 1000. Hence, a layer of 500-Å PSG can be used as the etch mask for 10,000 Å of poly-Si.

Stiction

Stiction During Release

The use of sacrificial layers enables the creation of very intricate movable polysilicon surface structures. An important limitation of such polysilicon shapes is that large-area structures tend to deflect through stress gradients or surface tension induced by trapped liquids and attach to the substrate/isolation layer during the final rinsing and drying step, a stiction phenomenon that may be related to hydrogen bonding or residual contamination. Recently, great strides were made towards a better understanding and prevention of stiction.

The sacrificial layer removal with a buffered oxide etch followed by a long, thorough rinse in deionized water and drying under an infrared lamp typically represent the last steps in the surface micromachining sequence. As the wafer dries, the surface tension of the rinse water pulls the delicate microstructure to the substrate where a combination of forces, probably van der Waals forces and hydrogen bonding, keeps it firmly attached (see Figure 5.17).[95] Once the structure is attached to the substrate by stiction, the mechanical force needed to dislodge it usually is large enough to damage the micromechanical structure.[84,94,95] Basically, the same phenomena are thought to be involved in room temperature wafer bonding (Chapter 8). We will not further dwell upon the mechanics of the stiction process here, but the reader should refer to the theoretical and experimental analysis of the mechanical stability and adhesion of microstructures under capillary forces by Mastrangelo et al.[96,97]

Creating stand-off bumps on the underside of a poly-Si plate[65,98] or adding meniscus-shaping microstructures to the perimeter of the microstructure are mechanical means to help reduce sticking.[99] Fedder et al.[100] used another mechanical approach to avoid stiction by temporarily stiffening the microstructures with polysilicon links. These very stiff structures are not affected by liquid surface tension forces and the links are severed afterwards with a high current pulse once the potentially destructive processing is complete. Yet another mechanical approach to avoid stiction involves the use of sacrificial supporting polymer columns. A portion of the sacrificial layer is substituted by polymer spacer material, spun-on after partial

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Volume 2: MICROMACHINING AND MICROFABRICATION

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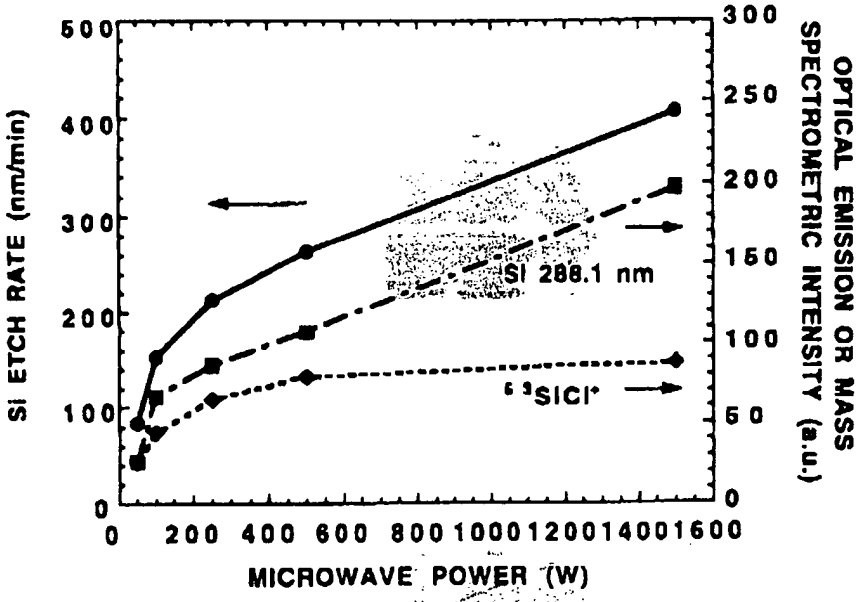

FIG. 3.11 Si etch rate, normalized Si emission signal at 288.1 nm (Si at 288.1 nm/Ar at 294.2 nm), and mass spectrometric $^{63}SiCl^+$ intensity as a function of microwave power. Samples were etched with 20 sccm of Cl_2 at 3 mTorr, 100 W rf power, and 8 cm below the ECR source.

microstructures, it is important that the Si etch rate be fast and the etch selectivity of Si over etch mask be high. The etch rate increased from 101 to 216 nm/min for rf power ranging from 50 to 300 W. Although high rf power is desirable for fast etch rate, the etch selectivity decreases with rf power. Figure 3.12 shows the durability of several etch masks in a Cl_2 plasma. Evaporated Ni was found to have higher selectivity than electroplated Ni, while thermal SiO_2 showed the lowest selectivity among the three etch masks. Evaporated Ni is not used as the etch mask because of its high intrinsic stress, which limits the thickness to <200 nm. The selectivity of evaporated and electroplated Ni decreased from 53 and 35 to 13 and 10, respectively, as rf power was increased from 50 to 300 W. Selectivity of SiO_2 was lower, decreasing from 9 to 7 within the same rf power range. This reveals that Ni is a more durable mask in Cl_2 plasma than SiO_2. There was a significant decrease in selectivity of Ni when rf power was increased from 50 to 75 W. This could be attributed to the threshold energy needed to sputter Ni. Although the selectivity is high at 50 W rf power, we did not apply this condition for our etches due to the slower etch rate. Within the range of rf power used, the Si etch profile is vertical and is independent of rf power.

Since feature size of different components on MEM devices varies substantially from 1 μm to several hundreds of micrometers, it is important to investigate how etch rate is influenced by feature size in order to provide

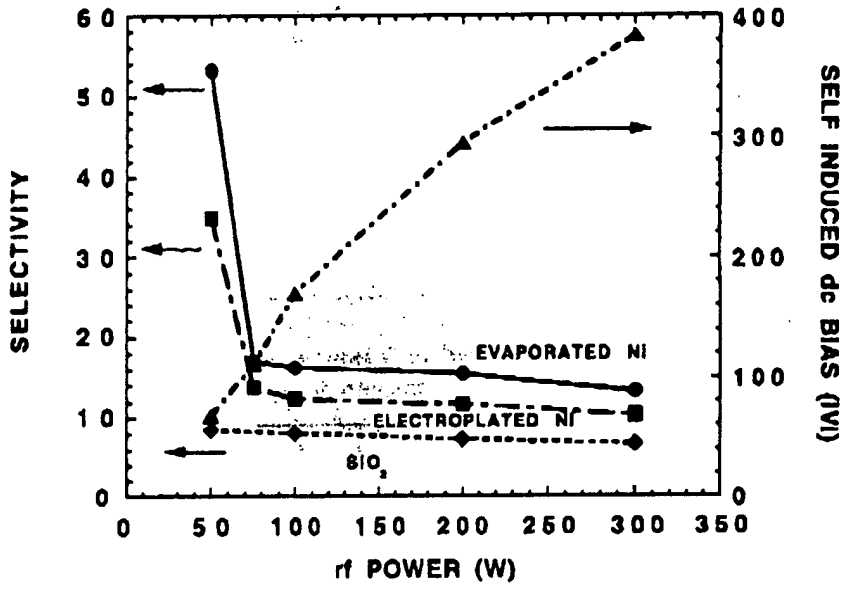

FIG. 3.12 Dependence of etch selectivity for evaporated Ni, electroplated Ni, and thermal SiO_2 etch masks on rf power. The Cl_2 plasma was generated by 100 W microwave power at 3 mTorr, a 20 sccm flow rate, and 8 cm below the ECR source.

sufficient overetch time. The dependence of etch rate on spacing between elements is shown in Fig. 3.13. The samples were 8 cm below the ECR source and were etched to a depth of 10 μm with 100 W microwave power, 100 W rf power, and 20 sccm of Cl_2 flow. The Si etch rate was normalized to the etch rate of 30 μm wide openings on the Si wafer. The normalized etch rate decreased from 1 to 0.95 and from 1 to 0.86 as trench width varied from 10 to 1.5 μm at 3 and 50 mTorr, respectively. The reduced etch rate for narrower features could be caused by decreasing concentration of reactive species at the bottom of trenches or by increasing difficulty of removing the etch products. At lower pressure, which corresponds to a shorter residence time at fixed flow rate, the etch rate reduction for high aspect ratio features is less significant. Reactive species encounter more collisions before reaching the samples at higher pressure. Therefore, the angular distribution of the reactive species is larger and more reactive species impinge on the sidewalls, resulting in a reduced etch rate for smaller features and a more prominent microloading effect. This is undesirable because a longer overetch time is needed for sensor fabrication. Since this effect could also be caused by the difficulty of removing etch products when aspect ratio is high, increasing flow rate to reduce the residence time could help to minimize the microloading effect. Nevertheless, we found there was only a slight reduction in microloading effect at higher flow rate under the etch conditions used.

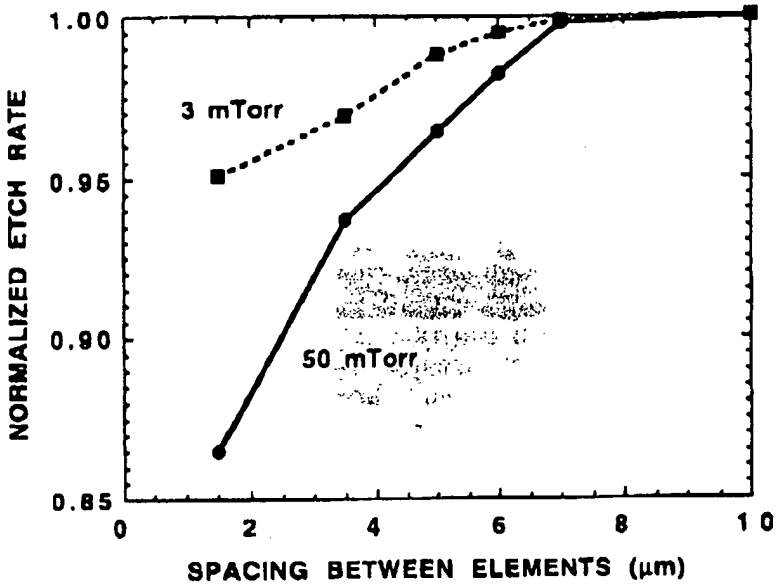

FIG. 3.13 Influence of spacing between elements on etch rate. Samples were etched with 100 W microwave power, 100 W rf power at 20 sccm Cl_2 and 8 cm below the source.

Si etch rate also depends on trench aspect ratio. Trench aspect ratio is defined as the ratio between the depth and the opening width of the trench. An average etch rate was obtained by dividing the trench etch depth by the total etch time, although the actual etch rate is faster at the initial stage and it slows down as the etch proceeds. For trenches with an aspect ratio >2, the average etch rate decreased linearly with aspect ratio, as shown in Fig. 3.14. The average etch rate was nearly constant for a trench aspect ratio ≤2. However, the etch rate started to decrease as the trench aspect ratio exceeded 2. The Si etch rate was 156 nm/min initially and it decreased to 119 nm/min for an aspect ratio of 34. For a trench aspect ratio ≥2, the Si etch rate can be fitted by R = 156 - A, where R is the average etch rate in nm/min and A is the trench aspect ratio.

Both etch rate and profile need to be controlled for Si microsensors with high aspect ratio elements. The effects of etch conditions on the etch rate and profile for deep Si microstructures are investigated. Pressure can have significant influence on the directionality of reactive species as well as the balance between etch and deposition reactions during dry etching. The Si etch rate for 2 μm wide openings was found to decrease from 151 to 124 nm/min as the pressure was increased from 3 to 30 mTorr, whereas the rate for 10 μm wide openings decreased from 163 to 141 nm/min. At lower pressure, the differences in the etch rate for the 2 and 10 μm openings are smaller. Lowering the pressure reduces the collisions of reactive species and etch products on the sidewalls. The ions are more directional and more ions can reach the bottom of narrow trenches since the number of collisions on the

sidewalls due to diverged ions is reduced. It is also easier, at lower pressure, for the etch species and products to move through deep trenches.

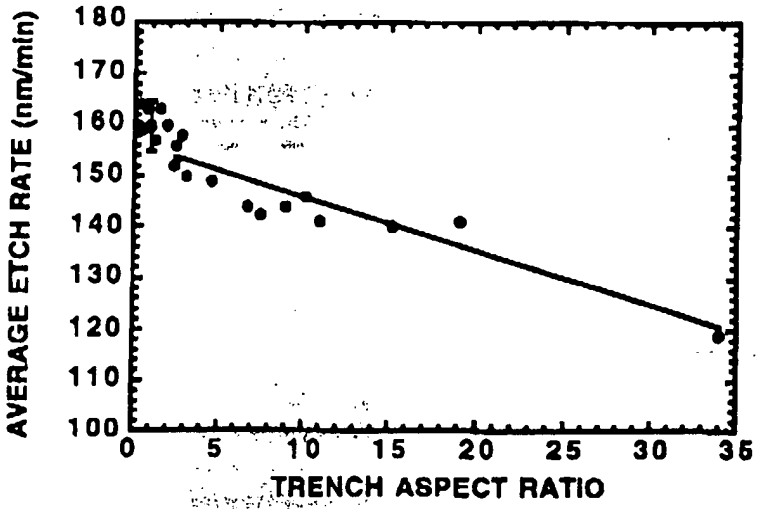

FIG. 3.14 Effect of trench aspect ratio on averaged Si etch rates for trenches with openings of 2, 3, 5, 20, and 50 μm. 100 W microwave power, 100 W rf power, 20 sccm of Cl_2, and an 8 cm source to sample distance at 3 mTorr were used.

Figure 3.15 shows the measured undercut widths as a function of pressure. The results are compared to those obtained using SPEEDIE simulation.[18] The samples were etched to a constant depth of 15 μm using 100 W microwave power, 100 W rf power, 20 sccm Cl_2, and an 8 cm source to sample distance. As the pressure was increased from 3 to 30 mTorr, the undercut width increased from 0.12 to 0.86 μm for 2 μm wide trenches and from 0.05 to 0.77 μm for 10 μm wide trenches. These results were similar to the undercut widths obtained using SPEEDIE simulations. For the Monte Carlo simulation, -160 V dc bias voltage, a 1 mm thick dark space sheath, and 1000 K of ion temperature were applied. Due to increased ion scattering at higher pressure, ions are less directional and more undercut is expected. The scattered species can impinge on the sidewalls and they can cause etching in the lateral direction. For narrower trench widths, collisions of diverged ions on the sidewalls are anticipated to increase further. However, with wider trenches, reactive species and etch products can move through the deep trenches more easily and with fewer collisions on the sidewalls by diverged particles. As a result, wider trenches have less undercutting and faster etch rates.

The effect of pressure on the directionality of ions was obtained from SPEEDIE simulations. For pressures ranging from 3 to 30 mTorr, the number of ions within 3° off normal of the wafer surface is approximately the same. Nevertheless, the number of ions at 30 mTorr is roughly an order of magnitude larger than that at 3 mTorr for larger incident angles. The wider ion angular distribution at higher pressure can cause increased etching in the

lateral directions. The results from these simulations agree with the measured undercut widths.

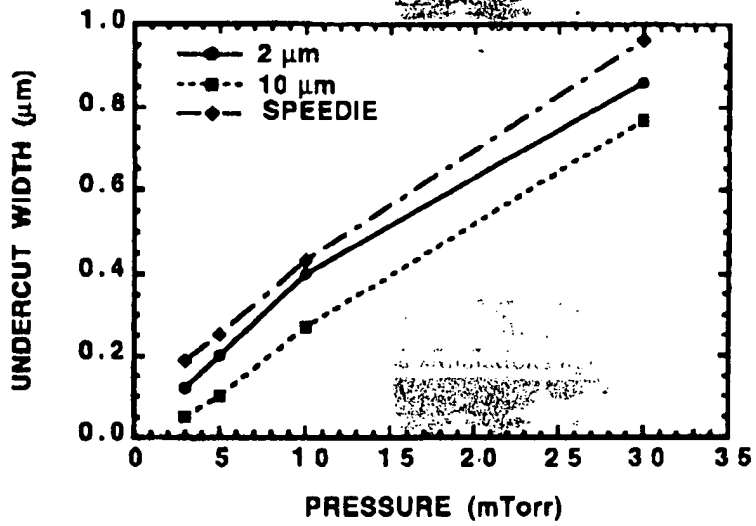

FIG. 3.15 Dependence of undercut width on pressure. The plasmas were generated with 20 sccm Cl_2, 100 W microwave power, 100 W rf power, and an 8 cm source distance. The etch depth was 15 μm.

By applying the optimized etch conditions, high aspect ratio microstructures in Si were obtained with 100 W microwave power, 100 W rf power, 20 sccm Cl_2 at 3 mTorr and 8 cm below the ECR source. Figure 3.16 shows Si resonators with an aspect ratio of 19. The etch depth is 28 μm, the spacing between elements is 1.5 μm, and the etched structures have a vertical profile and smooth morphology. The Si etch rate was 152 nm/min and it took 185 min to etch down to a depth of 28 μm. Even though etch rates can be increased by using higher microwave and/or rf power, they also result in an undercut etch profile and decreased selectivity, which are undesirable for etching of high aspect ratio microstructures. Further study is needed to increase the Si etch rate while still maintaining a vertical profile and high selectivity for etching sensing elements with a narrow gap and large depth. Despite the long etch time, these results show that by using a Cl_2 plasma generated by an ECR source, high aspect ratio etching of Si can be achieved and can be applied to the fabrication of MEM devices with higher sensitivity.

3.3.2 Deep Etch-Shallow Diffusion Technology

The bulk Si dissolved wafer process has been used to fabricate microstructures in single crystal Si.[19] In this process, a p^{++} etch stop layer is first formed by deep B diffusion. Microstructures are then fabricated by dry etching and released by wet etching of the Si substrate, stopping on the p^{++} layer. Since undercutting occurs during the conventional RIE step and a long diffusion time at high temperature is required to form a thick etch stop layer, the

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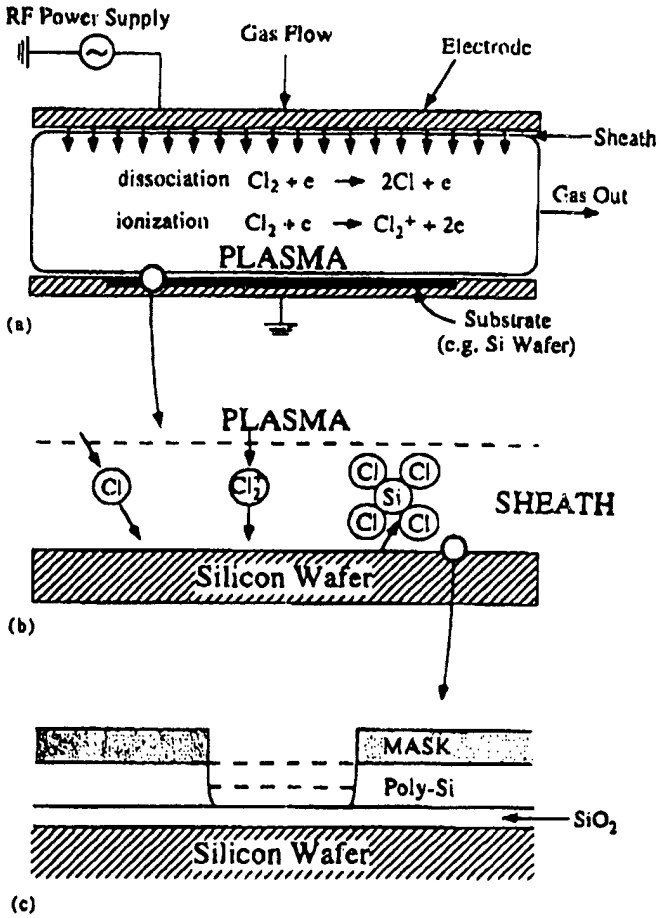

Figure 2 Operational characteristics of plasma etching. (a) Radicals and ions are generated in the plasma by electron impact of gas molecules. (b) The wafer is etched by the combined action of radicals and ions to yield a volatile product. (c) Ions accelerate in the sheath and bombard the wafer along the vertical direction, thereby inducing anisotropic etching of microscopic features. Dashed lines in (c) show the Poly-Si surface receding as a result of etching.

The goals of any plasma etch process are to achieve high *etch rate, uniformity*, and *selectivity*, controlled shape of the microscopic features etched into the wafer (degree of anisotropy), and no *radiation damage*. Manipulation of the plasma chemistry, coupled with the appropriate reactor design, is crucial for meeting these goals. There are many externally controlled variables that can

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Uniformity refers to achie
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Table 1 Comparison of W

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Selectivity
Resolution limit
Sidewall profile control
Waste disposal problem

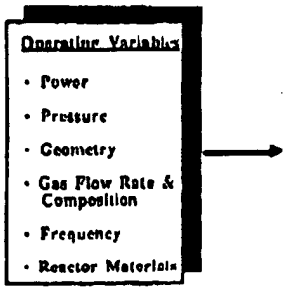

Figure 3 Representation of
plasma properties are the brid
of merit (process output).

influence the plasma chemistry, and in turn the process output. These are shown in Fig. 3.

High *etch rate* is desirable to increase the process throughput (wafers/hour). However, etch rate is often sacrificed to achieve better uniformity, selectivity, and anisotropy.

Uniformity refers to achieving the same etch rate across the wafer, which may be more than 20 cm in diameter. Nonuniform etching and/or nonuniformities

Table 1 Comparison of Wet and Plasma Etching

Characteristic	Plasma etching	Wet etching
Maturity	Industry standard	Industry standard
Cost	High	Low
Process control	Fairly easy	Not so easy
Etch rate	Moderate	High
Selectivity	Moderate	High
Resolution limit	<0.25 μm	>2 μm
Sidewall profile control	Good	Difficult
Waste disposal problem	Low	High

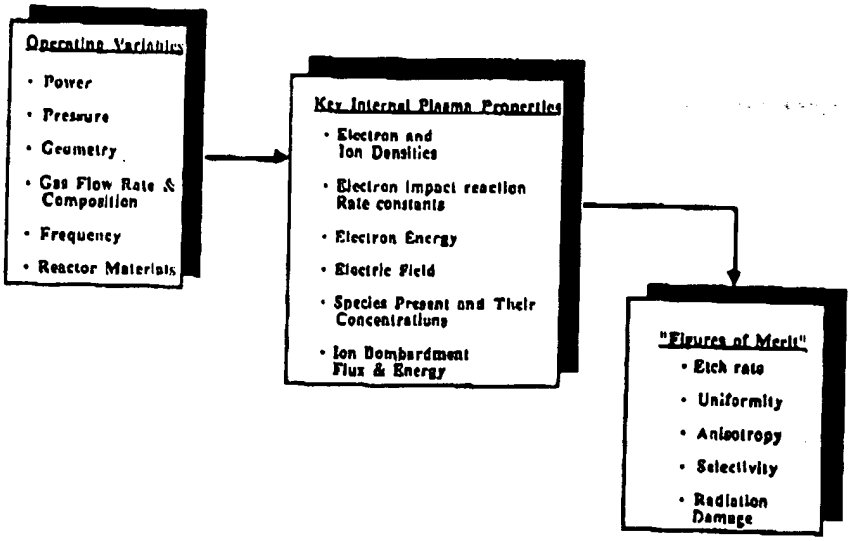

Figure 3 Representation of the parameter space in plasma etching. The key internal plasma properties are the bridge between externally controlled variables and the figures of merit (process output).

in the starting film thickness necessitate *overetch* beyond the *endpoint* of the process. Overetch must be minimized since the layer under the etched film (Fig. 1a) is then exposed to potentially harmful plasma radiation in some areas of the wafer while other areas are yet to clear. In addition, plasma uniformity is needed to avoid device damage (see below).

Selectivity refers to the relative rate of etching of one material with respect to another. Etch processes must be selective with respect to the mask and the underlying film. The mask must not be etched; otherwise, the desired pattern will be distorted. Selectivity with respect to the underlying layer is particularly important when that layer is thin or when the process uniformity is not good and overetch is required. For example, a process may call for etching polysilicon over a thin (100 Å) gate oxide. The selectivity of this process must be very high (>50:1); otherwise, a substantial thickness of the oxide may be lost.

The shape of the sidewall profile of the microscopic features etched into the wafer is of paramount importance. Most often anisotropic* sidewall profiles are required, perhaps with some taper at the bottom of the feature.

Radiation damage refers to structural damage of the crystal lattice or more importantly to electrical damage of sensitive devices caused by plasma radiation (ions, electrons, UV, and soft X-ray photons). For example, spatially nonuniform current flowing from the plasma to the wafer can lead to charging and breakdown of thin oxides; or intense ion bombardment can lead to structural damage of the top atomic layers of the etched film.

Plasma process development has been based largely on trial-and-error procedures guided by experience and intuition. A more rational selection of plasma etch chemistry and also of the appropriate plasma reactor design can be based on understanding the fundamentals of the chemical and physical processes taking place in the plasma and on the wafer surface.

In what follows, the fundamentals of plasma etching are discussed with emphasis on plasma chemistry. Discussion pertains to the kind of plasmas used in electronic materials processing. First, the general physical characteristics of plasmas are outlined. Gas-phase and surface chemistry are covered in some detail. Etching and chemical mechanisms for the most important material systems follows. The chapter concludes by discussing novel plasma etching systems.

Plasmas are also used for the low-temperature deposition of thin solid films. Reviews of plasma deposition can be found in Ref. 3.

*Literally speaking, anisotropic is anything not isotropic. In the plasma etching jargon, however, anisotropic etch is often taken to mean one with vertical or nearly vertical sidewalls.

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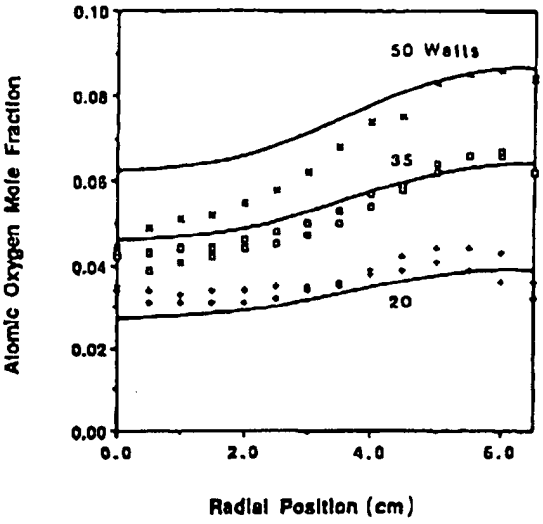

Figure 22 Atomic oxygen concentration, measured by optical emission actinometry, as a function of radius in a 13.56 MHz oxygen discharge sustained in a diode reactor. The electrode is covered with a reactive film up to a radius of 3.75 cm. This film acts as a sink for atomic oxygen, resulting in significant radial concentration gradients. Such gradients are responsible for etch nonuniformity. Solid lines show the result of mathematical model predictions. (From Ref. 18, with permission.)

and their concentration dips in that region. In contrast, the atom concentration builds up over the surrounding inert region. The gradient in the radical density thus established is most important around the periphery of the film. This gradient would lead to a so-called "bull's-eye" clearing pattern, whereby the etch rate decreases from the periphery to the center of the wafer. This "local" loading can be enhanced at higher power input to the plasma.

Loading can also occur at the microscopic feature scale (microloading). It has been observed, for example, that isolated features etch faster than dense patterns. This is due to local reactant depletion over the dense pattern caused by greater consumption of the reactant (greater etchable surface area exposed by the dense pattern). If reactant transport is not adequately fast to alleviate concentration gradients in the reactor, then loading can manifest itself.

6. Aspect-Ratio-Dependent Etching

Aspect-ratio-dependent etching (ARDE) refers to a situation commonly observed in etching of high-aspect-ratio (depth:width) features. It has been found that the etch rate decreases as the trench aspect ratio increases (also known as reactive ion etching, or RIE, lag). Figure 23 shows a typical situation. A combination

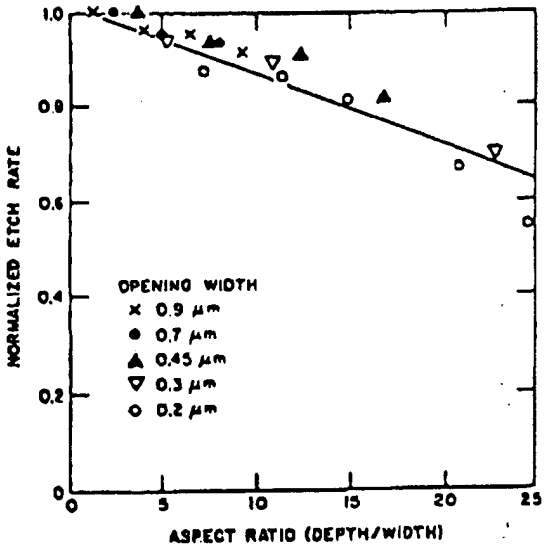

Figure 23 Aspect-ratio-dependent etching of silicon in a CCl_2F_2/O_2 gas mixture. The etch rate is a function of the aspect ratio of the feature (depth/width). (From Ref. 19, 1985 with permission.)

of effects can result in ARDE. As the feature becomes deeper, for example, ions may impact the sidewall instead of the feature bottom. This can be due to the angular distribution of the incoming ion flux, or the decollimation of ions due to electric fields developed by nonuniform charging of the mask or the feature sidewalls. As the flux of ions impinging on the feature bottom decreases, the etch rate follows suit. Also, transport limitations may reduce the flux of neutrals reaching the bottom of the feature for high-aspect-ratio features. One should not confuse ARDE with microloading. The latter can occur even for the same aspect ratio features. Finally, in a less common situation, the etch rate increases as the feature deepens (inverse RIE lag).

IV. PLASMA ETCHING SYSTEMS

Table 5 provides common examples of etching gases and the materials they etch. A brief discussion of several material systems is given below [11].

A. Silicon, Oxide, and Nitride

Silicon, silicon dioxide (oxide), and silicon nitride (nitride) are among the most important materials in microelectronics. Etching of these materials has tradi-

Table 5 Etching Gase

Source gas	Additive ga
CF_4	O_2
SF_6	O_2
SF_6	He
NF_3	None
C_2F_6	O_2
CF_4	H_2
NF_3	Cl_2
C_2F_6	CHF_3
Cl_2	Ar
Cl_2	C_2F_6
Cl_2	BCl_3
Cl_2	CCl_4
Cl_2	O_2
Cl_2	None
CCl_4	O_2
CH_4	H_2
O_2	H_2O

*SP = sidewall passivation

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$$R_{SiO_2} = 0.614 \times 1$$

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Preface

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DRY ETCHING FOR MICROELECTRONICS

Edited by

RONALD A. POWELL
Solid State Laboratory
Varian Associates, Inc.
Palo Alto, California, USA

1984

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beam milling (high resolution, anisotropy, independent control over process parameters) to produce a new dry etching technology capable of addressing the demands of LSI processing and the future, more stringent demands of VLSI processing.

Before describing the RIBE technique, therefore, we briefly review salient features of the dry etch techniques which preceded it and influenced its development.

2. Dry etch technologies

2.1. *Plasma etching*

In reactive plasma etching, substrates are directly exposed to a chemically-active, partially ionized gas. The composition of the etching gas is chosen to efficiently volatilize the layer to be etched and to provide good selectivity with respect to etch mask and underlying substrate. Usually, the etch gas chosen is chemically nonreactive in its neutral, ground state. Only upon entering the glow discharge region of the plasma where it is decomposed and ionized (into ions, electrons, free radicals, etc.) are reactive species available. The equipment used for this process falls into one of two generic types: the barrel reactor and the parallel plate or planar reactor.

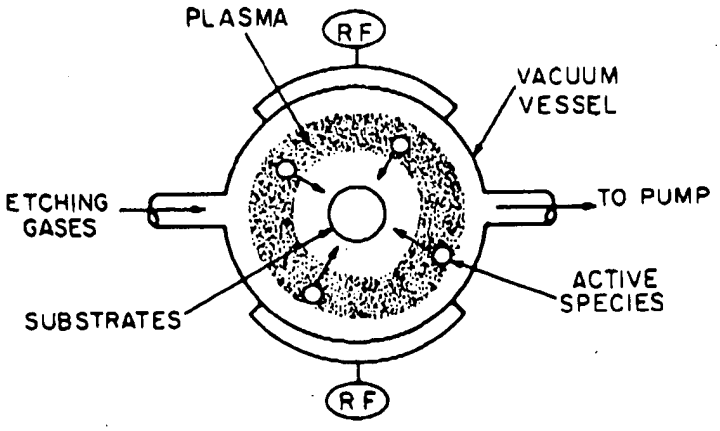

Fig. 1. Capacitively coupled barrel-type RF plasma reactor.

Figs. 14, 15, 38–42, 51–53 reprinted by permission of the publisher, The Electrochemical Society, Inc.; Figs. 8, 32 and 35 were originally presented at the Spring 1983 Meeting of the Electrochemical Society, Inc., held in San Francisco, California.

Figure 1 is an illustrati
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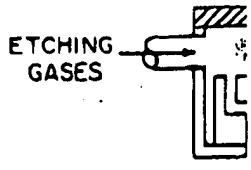

Fig. 2

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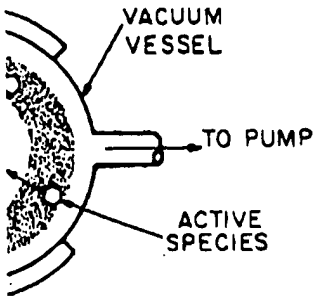


el-type RF plasma reactor.

Figure 1 is an illustration of a *barrel reactor*. Typically, a boat of wafers is placed in a perforated 'Faraday cage' held at ground potential. This cage is centered in a cylindrical vacuum vessel and RF power provided by capacitive (as shown) or inductive coupling. The vacuum vessel is evacuated to a base pressure between 100 mTorr and 1 Torr by a mechanical pump, at which point the appropriate etching gas is fed into the vessel in continuous flow to the vacuum pump. This gas is then decomposed and ionized in the chamber by RF energy. Neutral reactive species are then able to diffuse through the Faraday cage to react with those portions of the substrate not protected by resist. The etching in this case is entirely a chemical process. This technique provides, through the careful selection of reactive gas, excellent selectivity. The major disadvantage of the barrel reactor is that the etching is almost always isotropic. As with any 'pure' chemical process, it is also sensitive to impurities, both in the etch gas and on the wafers prior to etch. A 'de-scum' etch is often required to control surface contamination on the substrates. Other problems of etching with barrel reactors are: etch rate uniformity, temperature control, process reproducibility and end-point detection.

In fig. 2, the parallel-plate, *planar reactor* is represented. It usually consists of two parallel plates, with the power being supplied to the upper plate and the substrates loaded onto a cooled lower plate. The glow discharge is created between the two parallel plates. In this configuration, the plasma is in contact with the substrate, which is thus exposed to low-energy ion and electron bombardment. The advantages of this geometry are: good selectivity, the etching can be anisotropic, and there is better uniformity, reproducibility and temperature control than in the barrel reactor. The disadvantages are: smaller wafer capacity, more radiation damage effects (since the wafers are in contact with the plasma) and, in some cases, the etching may leave residues.

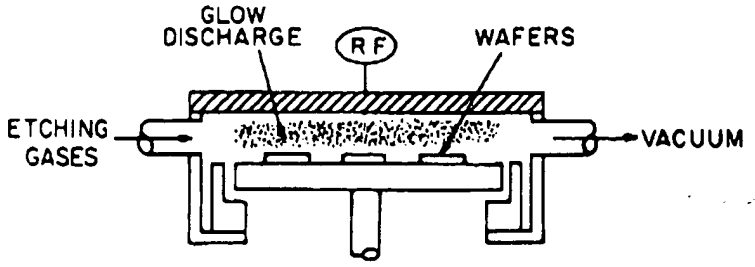
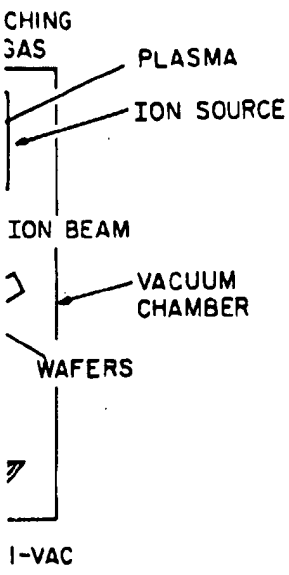


Fig. 2. Planar-type RF plasma reactor.



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technique, its instrumentation, and important applications in microelectronics. For additional reviews of RIBE, the reader is referred to references by Downey and Powell (1983), Bollinger (1983), Stein (1982), Hakhu (1981) and Downey et al. (1981).

3. Reactive Ion Beam Etching (RIBE)

3.1. General characteristics

Table 1 compares the operating characteristics of RIBE with other dry etch techniques. In RIBE, a gas capable of producing a reactive ion beam

Table 1
Comparison of operating characteristics of RIBE with other dry etch techniques.

Characteristic	Dry etch technique				
	Barrel etch	Planar plasma etch	Planar RIE	Ion beam milling	Reactive Ion Beam Etching
Substrate location	Surrounded by plasma	In plasma on grounded electrode	In plasma on driven electrode	In beam, separated from plasma	In beam, separated from plasma
Pressure	0.1–1 Torr	0.1–1 Torr	10-100 mTorr	$\sim 1 \times 10^{-4}$ Torr	$\sim 1 \times 10^{-4}$ Torr
Ion energy (eV)	0	10–100	100-700	300-1500	300-1500
Control of ion energy	None	Semi-independent	Semi-independent	Independent	Independent
Flux	Neutrals	Neutrals; low energy ions	Neutrals; high energy ions	Neutrals; high energy ions	Neutrals; high energy ions
Control of neutral flux	Independent	Semi-independent	Semi-independent	Semi-independent	Semi-independent
Selectivity	Excellent	Very good	Good	Poor	Good
Profile	Isotropic	Often isotropic	Often anisotropic	Anisotropic	Anisotropic
Degree of profile control	None	Low	High	None	Low
Reaction product	Volatile	Volatile	Nonvolatile & volatile	Nonvolatile	Nonvolatile & volatile
Mechanism	Chemical	Chemical	Physical & chemical	Physical	Physical & chemical

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- ☐ Maintenance Fee
- ☒ RCE
- ☐ Check No. _____ for $ 370.00

Atty/Secy DMC/tls

- ☐ TM Application ☐ ITU Basis
- ☐ Statement of Use
- ☐ Extension of Time
- ☐ Notice of Appeal
- ☐ Brief
- ☐ Petition
- ☐ Status Request
- ☐ Issue Fee
- ☐ Application for Renewal
- ☐ Specimen _____
- ☐ Certificate of Mailing
- ☐ Express Mail No. _____

PTO STAMP